#2 D.Duke 4-17-01

Form PTO-1449	APPLICANT: Magdy S. Abadir et al.	
LIST OF PATENTS AND PUBLICATIONS FOR INFORMATION DISCLOSURE STATEMENT (Use Several Sheets if Necessary)	ATTY. DOCKET #: SC11403TS	APPL. #: Unknown
	FILING DATE: Concurrently Herewith	GROUP: Unknown

C998 U.S. PTO 09/781492 02/13/01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,659,486	8/19/97	Tamiya	395	200.75	8/8/96
	AB	5,648,909	7/15/97	Biro et al.	364	488	6/12/95
	AC						
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	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE (#43)	COUNTRY	CLASS	SUBCLASS
	AL					
	AM					
	AN					
	AO					
	AP					

OTHER INFORMATION (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	Ringe et al., "Path Verification Using Boolean Satisfiability," Design, Automation and Test in Europe Conference & Exhibition, 2 pgs. (2000).
	AS	Liu et al., "Transistor Level Synthesis for Static CMOS Combinational Circuits," Ninth Great Lakes Symposium on VLSI Proceedings, 4 pgs. (1999).
	AT	Raimi et al., "Detecting False Timing Paths: Experiments on PowerPC™ Microprocessors," 36th Design Automation Conference Proceedings, pp. 737-741 (1999).
	AU	Lee et al., "Critical Path Identifiction and Delay Tests of Dynamic Circuits," IEEE, pp. 421-430 (1999), ITC International Test Conference.
	AV	Sivaraman et al., "Timing Analysis Based on Primitive Path Delay Fault Identification," IEEE, pp. 182-189 (1997), International Conference on Computer Aided Design.
	AW	Ashar et al., "Functional Timing Analysis Using ATPG," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 8, pp. 1025-1030 (Aug. 1995).
	AX	
	AY	
	AZ	

EXAMINER: _____ DATE CONSIDERED: 13-Dec-2002

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance *and* not considered. Include copy of this form with next communication to applicant.

#3 D. Duyn 4-12-01

INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT S/N 09/781,492 SC11403TS Magdy S. Abadir et al	
	FILING DATE 2/13/2001	GROUP Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	BA						
	BB						
	BC						
	BD						
	BE						
	BF						
	BG						
	BH						
	BI						
	BJ						
	BK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	BL							
	BM							
	BN							
	BO							
	BP							

OTHER INFORMATION

(Including Author, Title, Date, Pertinent Pages, Etc.)

	BR	Alfred L. Crouch, Design-for-Test for Digital IC's and Embedded Core Systems, 1999 by Prentice Hall PTR, pgs. 163-166.
	BS	
	BT	

EXAMINER	DATE CONSIDERED
	13-Dec 2002

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through the citation if not in conformance and not considered, and briefly state why citation was not considered. Include copy of this form with next communication to Applicant(s).

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